Implementation of Five Port Router Architecture Using VHDL

P. B. Domkondwar, Dr. D.S. Chaudhari

Abstract: Technology scaling continuously increasing number of component and complexity for System on Chip systems [1]. For effective global on-chip communication, on-chip routers provide essential routing functionality with low complexity and relatively high performance [1]. The low latency and high speed is achieved by allowing routing function for each input port and distributed arbiters which gives high level of parallelism [4]. This paper will provide an Design and implementation of on-chip router architecture.

Index Terms: Network on Chip Router, Round-Robin Arbiter (RRA), First In First Out (FIFO) Buffer, Finite State Machine (FSM).

I. INTRODUCTION

Network-on-Chip (NoC) design adopts data-routing network consisting of communication links and routing nodes to provide a shared, segmented global communication structure within the same chip. Wiring required to form communication links is very short because wires have to travel only local distance between routing nodes instead of global distances of an entire system. Therefore, scaling of data-routing network well with chip size and complexity is possible. The Network on Chip approach has a clear advantage over a traditional bus-based interconnect because of its layered and scalable architecture. [11].

The focus of this paper is on router, where on-chip router is the fundamental component of Network on Chip. For effective global on-chip communication, Network on Chip routers must provide essential routing functionality with low complexity and relatively high performance. The design goal of router is to provide the essential network functionalities while balancing performance and complexity.

II. DESIGN OF ROUTER

Fig.1 shows the block-level diagram of proposed router. The router has three main blocks, first-in, first-out (FIFO) buffer, crossbar switch and arbiter. The router is packet-switched and it provides five input/output ports to communicate with the local logic element and the neighboring routers. It receives the incoming packets and forwards them to the appropriate port. Buffers are present at various input ports to store the packets temporarily. Control logic will be present to take routing decisions and arbitration decisions. In proposed router store and forward methods of buffering has been chosen for the data flow. It has been chosen due to simplest possible decoding logic, thereby, reducing both area and power. Communication is done between output and input ports by use of two handshake signals (Req/Ack). The Req/Ack signals are used to access the FIFO buffer. Here, the crossbar switch is a very important component, the controls of which are maintained by arbitration logic control.

Fig.1 Block-level diagram of router
The crossbar switch directly connects the 5 inputs port to 5 outputs port of router with no intermediate stages.

In proposed architecture, data transfers by segmenting longer messages into smaller data packets, and forwarding these packets individually from sender to the receiver possibly with different routes and delays for each packet. Packets are composed of three fields, each field carrying specific information. Here packet size is of 40 bits. The first part is the header that contains three bit source address. Second part is destination address of three bit and remaining bits indicate payload portion in which user specify its contents.

III. FIRST-IN, FIRST-OUT BUFFER

In proposed router buffering is required to provide temporary storage of packets that are in transit. There is one input channel at each port, each running its own finite state machine (FSM) control logic. Each input channel has a first in first out (FIFO) buffer of depth 4 and data width of 40 bits and a control logic which has been implemented as a FSM. The FIFO FSM controller has role of receiving packet from the output port of the adjacent router and stores them in FIFO buffer and manages the flow control between adjacent router. The input channel accepts request from other neighboring router. On receiving the request, if it is free, it will acknowledge the request. Input channel will accept packet as long as the request signal is held high. The previous router’s output channel ensures that the request line is held high until it completely transmit the packet to input channel. Complete transmission of packet occurs if and only if FIFO buffer of that input channel is not full and width of the buffer storage and the on-chip interconnect equal to the packet size.

Fig.2 shows, first in first out (FIFO) buffer and its control logic. FIFO Buffer consist of FIFO control logic that control read and write operation of that corresponding input port. Reset and Clock signal is connected to FIFO Buffer.

When read signal (rd) or write signal (wr) to that input port is high then FIFO control logic performed read or write operation respectively for that port only. Read counter (cr) and write counter (cw) are the variables which stores number of read and write operation performed on that FIFO buffer. These variables are used to know whether the FIFO is empty or full. During read or write operation ready signal is low indicating, that particular channel is currently busy.

When read signal is high (rd=1), control logic first check fifoempty signal. If fifoempty signal is high it means FIFO is empty and no more data is available to performed read operation and operation is terminated. If fifoempty signal is low it means there is some data residing in FIFO memory, so packet is read from memory and read counter (cr) is incremented by one. When write signal is high (wr=1), control logic first check fifofull signal. If fifofull signal is high, it means memory is full and no more packets are added in it and operation is terminated. If fifofull signal is low, it mean FIFO memory is not full there is some space to store new arriving packet, so newly receiving packet can be write into the memory. Write counter (cw) is incremented by one. If read counter (cr) is equal to write counter (cw), it means number of read operation performed is equal to number of write operation, if write counter is equal to read counter then fifoempty (fe) signal becomes high which indicate that FIFO buffer is now become empty and fifofull (ff) signal becomes zero. If write counter is equal to four (cw=4), it means buffer became full and fifoempty (fe) signal became low and fifofull (ff) signal became high indicate that buffer is full.

IV. CROSSBAR

In proposed work the design of crossbar used five, 5:1 multiplexers. All five inputs are connected to all the multiplexers. Which input is forwarded to the output is decided by the select lines generated by the arbiter. Forty bit packets from all five input channel are apply as input to each multiplexers. Select line is of three bit generated by arbiter to select one of the multiplexer among five as output channel. Input to crossbar is 3bit select lines (SEL0 to SEL4) for five 5:1 multiplexers from crbmux0 to crbmux4. Another input is forty bit packets from input channel0 to input channel4 to each crossbar multiplexer. Thus every crossbar multiplexer having five forty bit packet as input. Output of every crossbar multiplexer depends on bits occurs on select lines of that particular crossbar multiplexer.
V. ARBITER

Arbiter controls the arbitration of the ports and resolves contention problem. It keeps the updated status of all the ports and knows which ports are free and which ports are communicating with each other. Packets with the same priority and destined for the same output port are scheduled with a round-robin arbiter. The arbiter will release the output port which is connected to the crossbar once the last packet has finished transmission. So that other waiting packets could use the output by the arbitration of arbiter. In proposed work, round robin arbitration algorithm use to assign priorities when many input ports request the same output. Output signal generated by arbiter is read, external clock, three bit select lines for crossbar switch to select output channel. External clock signals which is indication for next connecting router that data is now available on output port of source router. When it is high, it means data is now available on output port of that router. Read signals generated by considering current status of signal of that port only. Read signal is high only when fifoempty signal is low it means buffer is not empty, some data is store in it.

Arbiter generates three bit select lines to select output channel for outputting data out of router. Steps follow to generate three bit select lines to properly route incoming packet out of router given as below. First compare three bit destination address to select output channel for data flow out of router. Next three bit are source address indicate the input channel from where packet is transmitted.

VI. ROUND ROBIN ARBITRATION SCHEDULING

In proposed work, packets with the same priority and destined for the same output port are scheduled with a round-robin arbiter. To understand how the arbiter apply round robin arbitration scheduling to assign priority to different input channel requesting for same output channel, Assume if input channel0,2,4 are requesting for same third output channel. Then RRA scheduling use by arbiter, according which packet from input channel0 is outputted first through third output channel, after that packet from input channel2 is outputted through third output channel lastly packet from input channel4 is outputted through third output channel.

VIII. CONCLUSION

A light weight parallel router architecture for Networks-on-Chip is implemented on FPGAs. We implement optimizations in the FSMs and decoding logic, thereby, saving significant area. We intend to build an advanced router.

Fig. 3 Inter-router interaction during a packet transfer

Fig. 4 Round Robin Scheduling apply by router to transfer packets
REFERENCES


[10] A. Jantsch and H. Tenhunen,“Networks on Chips.”


**Priti B. Domkondwar** received her B.E. degree in Electronics and Telecommunication Engineering from Sant Gadage Baba Amravati University, Amravati in 2003, and she is currently pursuing the M.Tech. degree in Electronic System and Communication (ESC) at Government College of Engineering Amravati. She has around 6 years teaching experience. Her area of interest includes communication engineering. She has attended one day workshops on ‘VLSI & EDA Tools & Technology in Education’ and ‘Cadence-OrCad EDA Technology’ at Government College of Engineering Amravati.

**Devendra S. Chaundhari** obtained BE, ME, from Marathwada University, Aurangabad and Ph.D. from Indian Institute of Technology, Bombay, Powai, Mumbai. He has been engaged in teaching, research for period of about 25 years and worked on DSTSERC sponsored Fast Track Project for Young Scientists. He has worked at Head Electronics and Telecommunication, Instrumentation, Electrical, Research and incharge Principal at Government Engineering Colleges. Presently he is working as Head, Department of Electronics and Telecommunication Engineering at Government College of Engineering, Amravati. Dr. Chaundhari published research papers and presented papers in international conferences abroad at Seattle, USA and Austria, Europe. He worked as Chairman / Expert Member on different committees of All India Council for Technical Education, Directorate of Technical Education for Approval, Graduation, Inspection, Variation of Intake of diploma and degree Engineering Institutions. As a university recognized PhD research supervisor in Electronics and Computer Science Engineering he has been supervising research work since 2001. One research scholar received PhD under his supervision. He has worked as Chairman / Member on different university and college level committees like Examination, Academic, Senate, Board of Studies, etc. he chaired one of the Technical sessions of International Conference held at Nagpur. He is fellow of IE, IETE and life member of ISTE, BMESI and member of IEEE (2007). He is recipient of Best Engineering College Teacher Award of ISTE, New Delhi, Gold Medal Award of IETE, New Delhi, Engineering Achievement Award of IE (I), Nashik. He has organized various Continuing Education Programmes and delivered Expert Lectures on research at different places. He has also worked as ISTE Visiting Professor and visiting faculty member at Asian Institute of Technology, Bangkok, Thailand. His present research and teaching interests are in the field of Biomedical Engineering, Digital Signal Processing and Analogue Integrated Circuits.