Design and Simulation of 1-Bit Sigma–Delta ADC Using Ngspice Tool

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Abstract - This paper presents the design of a first order 1-bit sigma-delta oversampling analog-to-digital converter (ADC) which is realized using CMOS technology .Power consumption is the major issue in VLSI Design. In this paper an efficient low power first Order 1-bit Sigma-Delta ADC designed which accept input signal bandwidth of 10 KHz and a 5 MHz sampling clock frequency and implemented in a standard 0.18μm n-well CMOS process. The ADC operates at 2.5 reference voltage. The Simulation of design is done by using Ngspice Simulation Software[8]. This paper firstly elaborate about ADC types and Classification among Nyquist rates and Oversampling ADCs. Further, design of 1-bit Sigma Delta ADC is to be proposed which consists of Opamp as a key component in Sigma delta ADC. Opamp at integrator stage is with the open loop voltage gain 10,530V/V, Gain Bandwidth (GB) is 5MHz, output resistance is 122.5KΩ, and power dissipation is 0.806 mW. Finally, a first order 1-bit Sigma Delta ADC is implemented using ±2.5 power supply and simulation results are plotted using Ngspice tool.

Index Terms- 1-bit Sigma Delta ADC, CMOS Technology, Ngspice Tool

I. Introduction

The sigma delta conversion technique has been in existence for many years, but recent technological advances now make the devices practical and their use is becoming widespread. The converters have found homes in such applications as communications systems, consumer and professional audio, industrial weight scales, and precision measurement devices. The sigma-delta (Σ-Δ) ADC is now used in many applications where a low cost, low bandwidth, low power, high resolution ADC is required. [1]

The key feature of these converters is that they are the only low cost conversion method which provides both high dynamic range and flexibility in converting low bandwidth input signals. They are best suited for the slow and medium speed conversions such as instrumentation, digital voice and audio applications with conversion rate has entered into the megahertz range as high as possible 15 bits of resolution.

Sigma delta (Oversampling)analog to digital converter based on oversampling method .it uses high frequency modulation and thus eliminates the need for anti-aliasing filters at the input to ADCs like Nyquist rate ADCs Compared with other ADCs the analog circuitry of Sigma-Delta ADC (Σ-Δ ADC ) is simpler and easier to be realized[1][6].

An Σ-Δ ADC contains very simple analog electronics (a comparator, voltage reference, a switch, and one or more integrators and summing circuits) and quite complex digital computational circuitry this circuitry consists of a digital signal processor (DSP) which acts as filter. In this project, design of Σ-Δ ADC with 0.18μm CMOS technology .The ADC uses the Op-amp to design of integrator and comparator at an operating power supply of ± 2.5v .The Final Circuit is constructed and simulated using Ngspice simulation tools.

II. Basics of ADCs

An analog-to-digital converter (A/D) is a device which converts continuous quantity to a discrete time digital
The basic ADC function is shown in Figure 1 above. This could also be referred to as a quantizer. Most ADC chips also include some of the support circuitry, such as clock oscillator for the sampling clock, reference (REF), the sample and hold function, and output data latches. In addition to these basic functions, some ADCs have additional circuitry built in. These functions could include multiplexers, sequencers, auto-calibration circuits, programmable gain amplifiers (PGAs), etc.

III. Types of ADCs

ADCs can be separated into two categories depending on the rate of sampling. The first category samples the input at the Nyquist rate, or \( f_N = 2F \) where \( F \) is the bandwidth of the signal and \( f_N \) is the sampling rate. The second type samples the signal at a rate much higher than the signal bandwidth. This type of converter is called an oversampling converter. The oversampling ADC is able to achieve much higher resolution than the Nyquist rate converters. The accuracy of the converter does not depend on the component matching, precise sample-and-hold circuitry, or trimming, and only a small amount of analog circuitry is required. However, because of the amount of time required to sample the input signal, the throughput is considerably less than the Nyquist rate ADCs.

A. Nyquist-Rate ADCs

- Flash ADCs
- Sub-Ranging ADCs
- Folding ADCs
- Pipelined ADCs
- Successive Approximation (Algorithmic) ADCs
- Integrating (Serial) ADCs

B. Oversampling ADCs

- Delta-Sigma based ADCs

Figure 2. Comparison of all ADCs according to resolution (Bits) and sampling rate (samples/s) [7]

IV. Classification of ADCs architectures

<table>
<thead>
<tr>
<th>Type</th>
<th>Nyquist ADCs</th>
<th>Oversampled ADCs</th>
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<tbody>
<tr>
<td>Slow</td>
<td>Integrating (serial)</td>
<td>Very high resolution &gt;14-bits</td>
</tr>
<tr>
<td>Medium</td>
<td>Successive approximation</td>
<td>Moderate resolution &gt; 10-bits</td>
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<tr>
<td></td>
<td>(1-bit pipeline architecture)</td>
<td></td>
</tr>
<tr>
<td>Fast</td>
<td>Flash (Multiple-bit pipeline)</td>
<td>Low resolution &gt; 6-bits</td>
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V. 1-bit Delta-Sigma Converter

Figure 3. 1bit Delta-Sigma ADC implementation [5]
Figure shows the block diagram of a proposed first order Delta-sigma Converter (Σ-Δ ADC). It consists of Integrator, a comparator (1 bit ADC), D-latch, 1-bit DAC. In above circuitry a 1-bit ADC (generally known as a Comparator), drive it with the output of an integrator, and feed the integrator with an input differenced with the output a 1-bit DAC fed from D-latch output.

VI. Circuit Description

The integrator is simple Miller integrator using a large resistor and small capacitor to minimize layout space. The values of the resistor and the capacitor decide the time constant of the integrator. The time constant shouldn’t be too big. Otherwise, the integrator will go into saturation status. Op-amp is the core part of the sigma delta converter. It provides a large open loop gain to integrate smoothly. The output of integrator feeds to the input of a comparator referenced to ground to quantize this signal to VDD or VSS. This output is then fed to a D flip-flop, which inserts the necessary delay to clock the circuit. The output of this is fed into a DAC reference level adjustment which converts this back to dynamic range of the input signal. The DAC operates from the Q and Q bar outputs of the flip-flops. The sum at the input to the Miller integrator is a negative sum because the DAC output is negatively referenced. The summing resistance values are equal to assign an equal weight to both parts in the integration. The following sections detail the design aspects of each circuit component.[4]

VII. Op-amp Design

The operational amplifier that the integrator uses must have the high gain to effectively carry out a smooth integration as well as a large enough bandwidth to support the high frequency sine waves it will be integrating. The op amp operates at the clock frequency, since the differences are being integrated over the region of time. Therefore, the gain bandwidth product of the opamp must be greater than one at the clock frequency to effectively pass the signal. The amplifier used is shown in figure. The key thing to note to about the amplifier is the frequency compensation network which is used to push the high frequency zero out of the pass band of the opamp. The Frequency response of Op-Amp is shown below. The open loop voltage gain is 10,530V/V, Gain Bandwidth (GB) is 5MHz, output resistance is 122.5KΩ, and power dissipation is 0.806 mW. Phase margin for 10pF load is 65° and the open loop output voltage swing is +2.3 to -2.2 V.

Figure 4. The Op-amp Design using CMOS [3]

Figure 5: The frequency response of op-amp (magnitude and phase plots)

VIII. Comparator Design

The 1-bit Sigma Delta consists of a 1-bit ADC which is composed of a comparator and a D-flip-flop. The design of comparator is similar enough to that of an Op-amp. The only difference is the use of the compensation network consists of resistor and capacitor and extra multipliers on a biasing NMOS device. The comparator does not need the compensation network because its only function is to switch from rail to rail. Stability is not needed as it will only slow down the switching speed. When a sine wave is input to the circuit, the comparator switches from positive rail to negative rail. The propagation delay of the comparator is 5ns.
IX. Flip-Flop Design

The D flip-flop is composed of two D latches arranged in a master–slave configuration. Each D latch consists of two transmission gates and two inverters. The outputs Q and Qbar are taken off the outputs of the second D latch B and Bbar respectively. The clock frequency of D flip-flop decides the sampling rate. In this case, D flip-flop operates at 5 MHz.

X. 1-bit DAC Design

The DAC consists of two transmission gates and two pairs of resistors. The input to each transmission gate is a voltage divided down from the positive and negative 2.5 volt rails which acts as ±Vref signals depending on the 1-bit digital input signal. In the operation of the sigma–delta modulator, the DAC receives a square wave signal from the flip-flop. In the feedback path, the DAC shifts the logic level so that the feedback term matches the logic level of the input; making the difference equally weighted.
XI. Simulation Result of 1-bit Sigma Delta ADC

The circuit design of first order Sigma-Delta (Σ-Δ ADC) have been developed and implemented by using 0.18um CMOS technology. The whole First order Sigma-Delta ADC system works very well under the following conditions.

Input sine wave frequency up to 10 KHz
Clock frequency (D-Latch) 5MHz

The output signal of converter is a pulse density waveform. Figure 10 shows the input and output of (Σ-Δ) ADC modulator.

![Input and Output results of 1-bit Σ-Δ ADC](image)

Figure 10. The Input and Output results of 1-bit Σ-Δ ADC

XIII. References

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